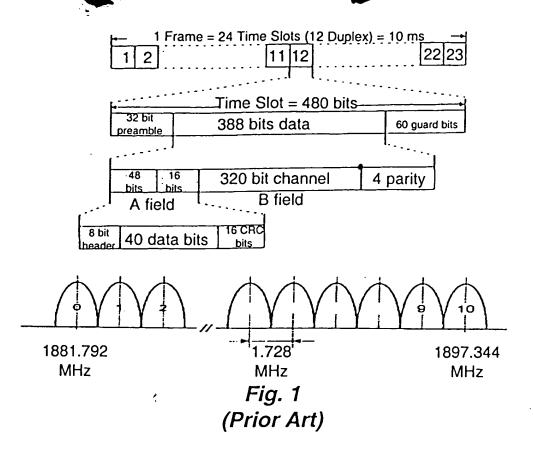
_|



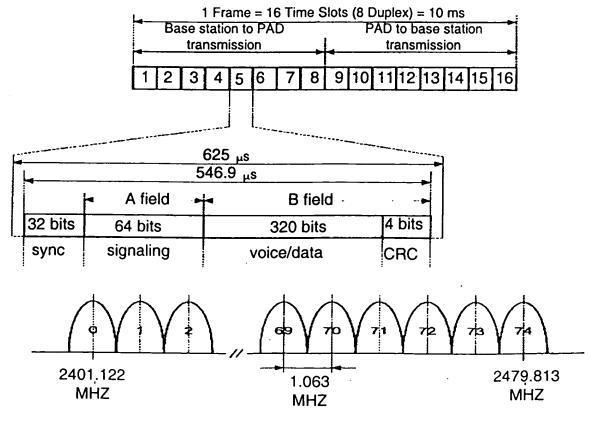


Fig. 7

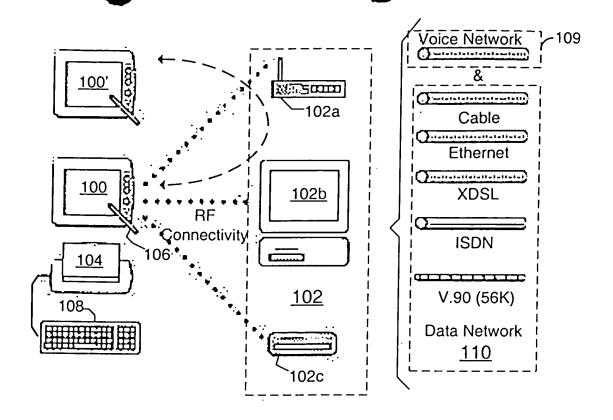


Fig. 2

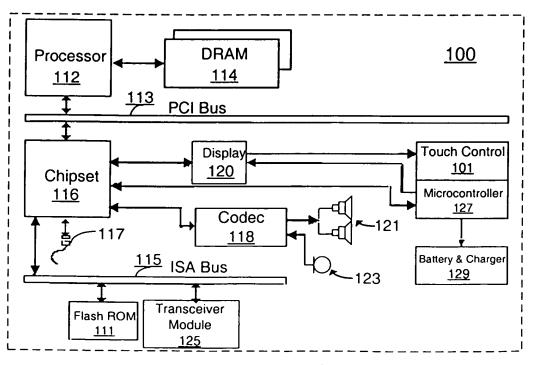


Fig. 3

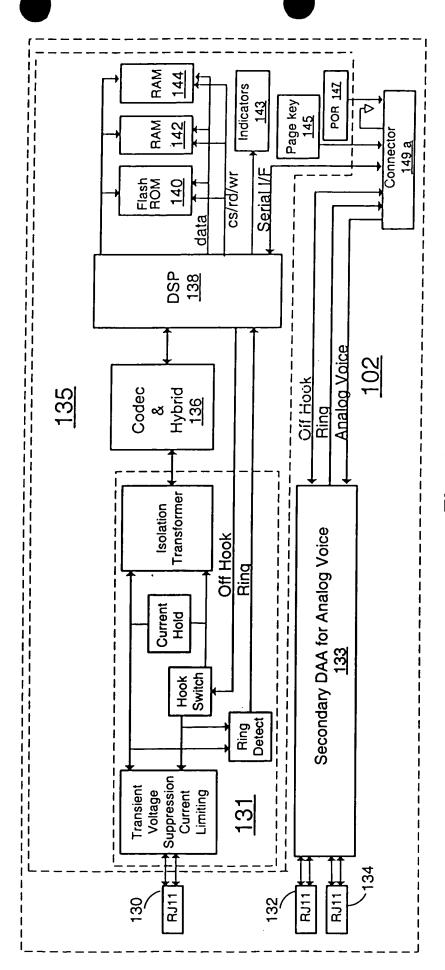


Fig. 4

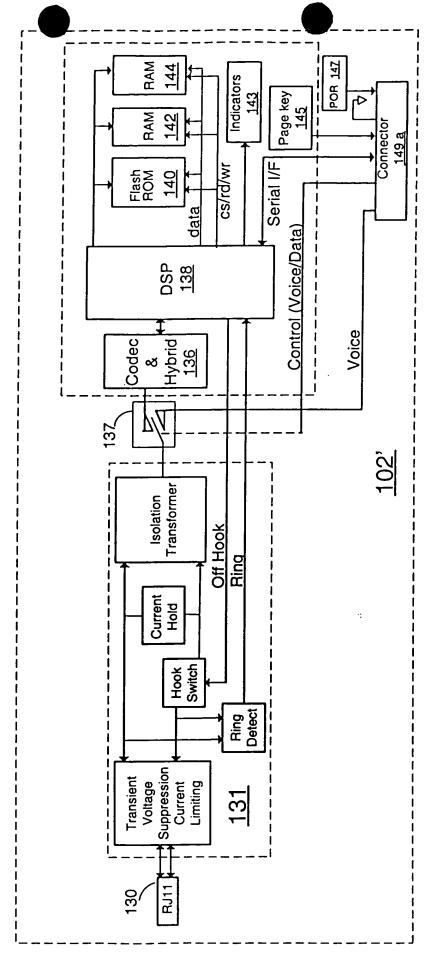


Fig. 5

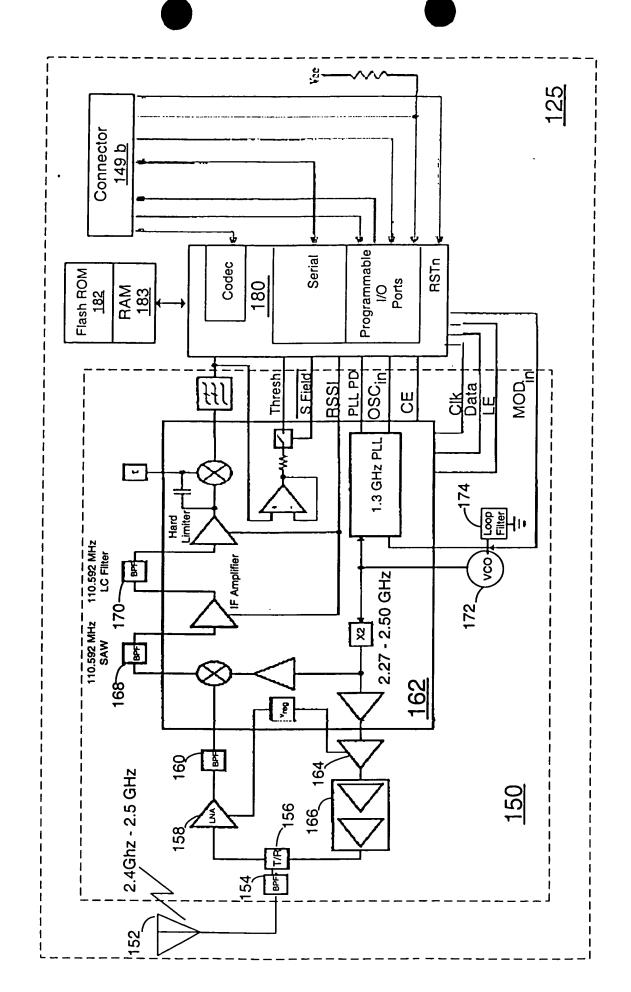
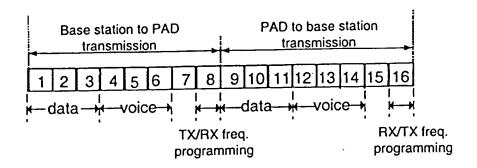


Fig. 6



		625 rs					
546.9μS							
l l i	A field		B field				
32 bits	64 bits	80 bits	240 bits	4 bits			
sync	signaling	FECC	data	CRC			

	62	25 rs	
4	54	6,9µ\$	
ř	A field	B field	·•
32 bits	64 bits	320 bits	4 bits
sync	signaling	voice	CRC

Fig. 8

PREAMBLE		HEADER			DATA		
SYNC WORD 80 BITS	FRAME TIMING 16 BITS	DATA WORD LENGTH 12 BITS	DATA RATE 4 BITS	ERROR CHECK WORD 16 BITS	DATA 1-4095 BYTES		
128 ВПЅ —							

Fig. 9 (Prior Art)